CLAIMS

What is claimed is:

1. A circuit having a class-AB output stage, comprising:

first, second, third, and fourth MOS transistor devices configured in a translinear loop, the first MOS device carrying a first control current, the second MOS device carrying a second control current, the third MOS device carrying a current equal to the sum of the first and second control currents, and the fourth MOS device carrying a bias current;

a first output circuit coupled to a first voltage supply and an output node, the first output circuit sourcing a first output current based on the first control current; and

a second output circuit coupled to a second voltage supply and the output node, the second output circuit sourcing a second output current based on the second control currents.

2. The circuit of claim 1 wherein the first and second output circuits are current mirrors and the first and second output currents equal the first and second control currents, respectively.

3. The circuit of claim 1 wherein the MOS devices are NMOS devices.

4. The circuit of claim 1 wherein the MOS devices operate in weak inversion mode.

5. The circuit of claim 1, further comprising a supply voltage having a voltage lower than $2 * V_{GS} + V_{DS}^{sat}$ to provide the first voltage supply.

6. The circuit of claim 1, further comprising a supply voltage having a voltage equal to $V_{GS} + 2* V_{DS}^{sat}$ to provide the first voltage supply.

7. The circuit of claim 1 wherein the bias current is programmable to permit user selection of a bias current.

8. The circuit of claim 1 wherein a quiescent current of the output stage is set by the bias control current, the bias current being increased above a selected predetermined level to lower a distortion level of the circuit.

9. The circuit of claim 8, further comprising an audio circuit wherein the output node is coupled to the audio circuit.

10. A circuit having a class-AB output stage, comprising:

a plurality of MOS transistor devices configured in a translinear loop to generate first and second control currents having a harmonic mean relationship;

a first output circuit coupled to a first voltage supply and an output node, the first output circuit sourcing a first output current based on the first control current; and

a second output circuit coupled to a second voltage supply and the output node, the second output circuit sourcing a second output current based on the second control currents.

11. The circuit of claim 10 wherein the first and second output circuits are current mirrors and the first and second output currents equal the first and second control currents, respectively.

12. The circuit of claim 10 wherein the MOS transistor devices are NMOS devices.

13. The circuit of claim 10 wherein the MOS devices operate in weak inversion mode.

14. The circuit of claim 10, further comprising a supply voltage having a voltage lower than $2 * V_{GS} + V_{DS}^{sat}$ to provide the first voltage supply.

15. The circuit of claim 10, further comprising a supply voltage having a voltage equal to $V_{GS} + 2* V_{DS}^{sat}$ to provide the first voltage supply.

16. The circuit of claim 10 wherein the first voltage supply is 1.8 volts and the second voltage supply is a ground reference.

17. The circuit of claim 10 wherein the first and second output circuits comprise first and second output MOS devices, respectively, the maximum output voltage range at the output node being substantially equal to the difference between the first and second voltage supplies minus a saturation voltage of the first and second MOS output devices.

18. The circuit of claim 10 wherein the plurality of MOS transistor devices comprise first, second, third and fourth MOS transistor devices wherein the first MOS transistor device is coupled to the first control current, the second MOS transistor device is coupled to a current that equals in the sum of the first and second control currents, the third MOS transistor device is coupled to the second control current, and a forth MOS transistor device is coupled to a bias control current.

19. The circuit of claim 18 wherein the sources of the second and third and MOS devices are coupled to a bias voltage.

20. The circuit of claim 10 wherein a quiescent current of the output stage is set by a bias control current.

21. The circuit of claim 20, further comprising an audio circuit wherein the bias current is increased above a selected predetermined level to lower a distortion level of the circuit for use with the audio circuit.

22. The circuit of claim 20, further comprising a power control circuit wherein the output node is coupled to the power control circuit.